강의계획서

1. 교과목 개요

가. 교과목명 (학수번호, 이수구분 등) : 논리회로및실험

나. 담당교수 : 한현구

다. 교과목 학습목표: Analysis and synthesis of synchronous logic circuits using various flip-flops. Building logic circuits using registers and counters. Understanding the configurations of memories.

라. 강의 방법 및 자료 매체 (판서 모니터, PPT, 워드문서, 인터넷 등): PPT and 판서

마. 교재 및 참고문헌 : Digital design with an introduction to the Verilog HDL,
M. Morris and M. Ciletti

2. 주차별 수업 운영 계획(중간.기말고사 제외)

주 차 (week)	강의범위 및 내용 (contents)	비 고 (further information)
1	Combinational logic circuits review	
2	Flip-flops: S-R and D flip-flops	
3	Level and edge triggering, J-K and T flip-flops	
4	Analysis of clocked sequential circuits	
5	Analysis of clocked sequential circuits and HDL	
6	Introduction to Verilog Hardware Design Language	
7	State reduction and assignment, design procedures	
8	Sequential logic circuit design using various examples	
9	Registers: register with parallel load, shift registers	
10	Ripper counter, binary counter, BCD counter	
11	RAM, memory decoding, error detection and correction	
12	ROM, programmable logic array	
13	Register transfer level: Algorithmic State Machine(ASM)	
14	Binary multiplier, Control logic design using HDL	