강 의 계 획 서(Syllabus)

[1] 기본 정보(Basic Information)

■ 강의 정보(Course Information)

교과목명 (Course Title)	컴퓨터구조	강의유형 (Course Type)	단독강의

[2] 학습 목표/성과(Learning Objectives/Outcomes)

■ 과목 설명(Course Description)

This course covers computer organization and design. It provides students understanding of a CPU at a logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered. Hardware support for exceptions, dynamic scheduling of instructions, and branch prediction are also discussed. Computer arithmetic, memory hierarchies, and hardware-software interface are also covered.

■ 학습 목표(Learning Objectives)

The objective of this course is to introduce the design concepts used in computer architectures to improve the performance of computations. Performance improvement techniques employed at instruction set, gate, register transfer, processor, memory, I/O and multiprocessor design levels will be explored to achieve the objective.

■ 학습 성과(Learning Outcomes)

Students will learn knowledge about computer architectures and performance improvement techniques. At the end of the course, students are expected to feel confident to perform logic design of CPU structures or other hardware systems utilizing pipelining and other RTL techniques.

[3] 강의 진행 정보(Course Methods)

■ 강의 진행 방식(Teaching and Learning Methods)

강의 진행 방식	추가 설명
강의	

■ 수업 자료(Textbooks, Reading, and other Materials)

수업 자료	제목	저자	출판일/게재일	출판사/학회지
주교재(Main Textbook)	Computer Organization and Design ? The hardware / software interface	Patterson and Hennessy	2013	Elsevier

[4] 수업 일정(Course Schedule)

차시	강사명	수업주제 및 내용	제출 과제	추가 설명
1	백정엽	[Chapter 4] the processor : control design		

2	백정엽	Q&A session for Chapter 1~3		
3	백정엽	[Chapter 4] the processor : summary of single-cycle datapath and concept of pipelining		
4	백정엽	[Chapter 4] the processor : pipelined datapath (1)		
5	백정엽	[Chapter 4] the processor : pipelined datapath (2)		
6	백정엽	[Chapter 4] the processor : hazards, forwarding, summary		
7	백정엽	[Chapter 5] memory hierarchy: intro		
8	백정엽	[Chapter 5] memory hierarchy: disks and caches (1)		
9	백정엽	[Chapter 5] memory hierarchy: caches (2)		
10	백정엽	[Chapter 5] memory hierarchy: caches (3)		
11	백정엽	[Chapter 5] memory hierarchy: error correcting code and virtual memory		

[5] 수강생 학습 안내 사항